Multistacked Buck-Boost Converter for Partially Shaded Photovoltaic Module

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ABSTRACT

The photovoltaic (PV) string comprising of multiple modules / panels when subjected to partial shading condition creates multiple Maximum Power Points (MPPs) which makes its PV characteristic complex and limits the power generated. Thus, the investigation is done to maximize the PV generated power even when the PV string is subjected to partial shading. A single switch voltage equalizer which improves the power generated is proposed in this paper. The proposed voltage equalizer simplifies the circuit in comparison with the conventional voltage equalizer. The system is modeled using MATLAB-SIMULINK were the three PV panels/modules are connected in series.

KEY WORDS: Photovoltaic string, Partial Shading, Maximum Power Point, Voltage Equalizer.

1. INTRODUCTION

The solar energy is renewable, clean and green energy resource which plays a significant role in world energy in future. Solar energy is sun's radiant energy which can be converted directly into electrical energy with the help of solar cells and this phenomenon is called PV effect. The electrical energy obtained by this method has no harmful impact on environment. The solar irradiance, cell temperature, tilt angle shaded condition and the operating condition are the factors which influences the output current and power characteristics of PV module. The amount of incident light falling on the PV panel will determine the total generation charge carrier and thus the generated current in the PV panel.

The Photovoltaic technology has significantly increased worldwide in the previous years, with the application ranging from small rooftop i.e. kV to power plant i.e. MVA and at all kinds of installation location from rural spaces to residential area. In urban spaces, due to the mixture of installation location often leads to function at non-uniform illumination condition because of nearby obstacles which creates partial shading.

The partially shaded condition is said when one/more of PV modules in the array received less amount of solar irradiance. The block diagram and the waveform for partial shaded condition are shown in Fig.1.

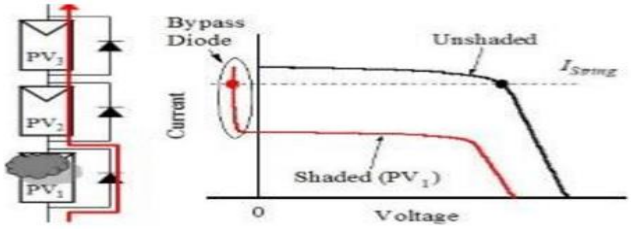

Figure.1. The block diagram and the waveform for partial shaded condition

When PV modules/panels is under partially shaded condition, the module characteristics becomes more complex due to the multiple local and global MPP's, MPP's is a unique operating point of the PV system at which maximum power is produced at optimum voltage and current.

The happening of multiple MPP's generally might cause PV modules to be trapped at the local MPP. At this working state, PV modules will generate lesser output power. The PV modules which operate at the absolute MPP can achieve higher power efficiency compared to the trapped local MPP.

The presence of multiple MPP's reduces the efficiency of MPPT algorithm since the power loss of PV system under partially shaded condition is high.

There is different maximum power point tracking algorithm such as perturb and observe (P&O), incremental conductance (IC) method. Out of which incremental conductance method is used for maximum power point tracking as it has less oscillation compared to perturb and observe method which results in higher efficiency.

For resolving partial shading issue most of the paper used distributed MPPT (DMPPT) instead of global MPPT. The string characteristics are shown with and without partial shading in Fig.2.

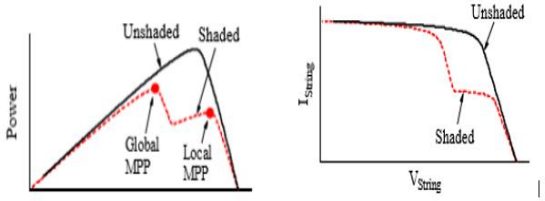

Figure2.The string characteristics is shown with and without partial shading

DMPPT means each PV module will operate at each MPP. However, the number of PV module is proportional to number of converters thus increases the number of modules required and makes the system costly and complex. Thus, an alternate powerful solution to this problem is voltage equalizer which will transfer a fraction of generated power from unshaded substring to shaded substring thus all substrings operates at same voltage.

Equalization Strategy:

General Description of voltage equalizer: There are various kinds of voltage equalizer proposed and developed. In a circuit, switch count in a converter can tell the complexity of the circuit. A gate driver circuit with a driver IC, auxiliary power source and ancillary components are required for each switch. In the case of bidirectional converters more than one switch is required per substring. And with the multi-winding flyback converter which simplifies the circuitry as only one switch is required per substring.

General Description of proposed voltage equalizer: In this paper a multi-stacked buck-boost converter with single switch voltage equalizer which is derived by stacking multiple capacitor-inductor-diode filter on traditional buck- boost converters using two inductors are proposed. This simplifies the circuit in comparison with the different voltage equalizer proposed as only one switch is required for any number of modules/substring. However, for this equalizer to work optimally, an equalization current supplied to unshaded modules must be controlled to be nearly zero, requiring multiple current sensors in proportion to the number of modules connected in series which increases cost and complexity of the circuit. Thus a current sensorless voltage- based control is preferable to the current-based one. The current sensorless equalization strategy reduced cost and simplified measurement circuit as well as decreased processed power and power conversion loss in the equalizer.

A block diagram of the proposed single-switch voltage equalizer for a string comprising three substrings of PV1-PV3 is shown below in Fig.3.

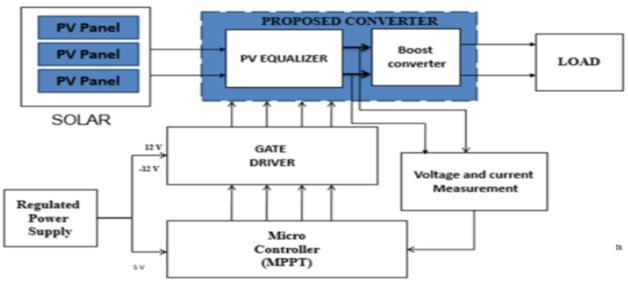

Fig 3. The block diagram of the proposed system

Equalizer circuit: The circuit diagram of the proposed equalizer is shown below in Fig.4.

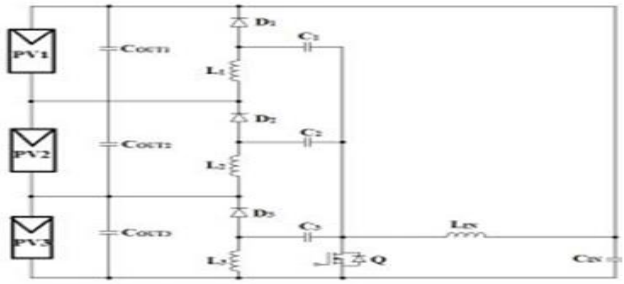

Figure.4. The circuit diagram of the proposed equalizer

The three PV modules PV1–PV3 connected in series and the output smoothing capacitors Cout1–Cout3 are connected in parallel with PV1–PV3, respectively. A fraction of the generated power of the string is fed to the input of the equalizer. Then, this supplied power is redistributed to shaded modules so that all module voltages are equalized. C-L-D filters are ac-coupled, suggesting that although PV1–PV3 are at different DC voltage levels, these C-L-D-filters as well as PV1–PV3 can be separated and grounded. All the C-L-D filters as well as PV1–PV3 are equivalently connected in parallel, and therefore, the equalizer preferentially supplies an equalization current to the module having the lowest voltage in a string. In general, a voltage of shaded modules tends to be lower than that of unshaded modules. Hence, equalization currents automatically flow toward shaded modules so that all the module voltages become nearly uniform. The single-switch equalizer operates in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the degree of shading. When degree of shading is high i.e. severely shaded then the operation falls on CCM on the other hand, when the degree of shading is light, the operation likely falls into DCM. When PV2 and PV3 are moderately and severely shaded, during T_{ON} period, the switch Q is turned on, and all the inductor currents, i_{Lin} and i_{L1}–i_{L3}, linearly increase and flow through Q, as shown in Fig. 8. Voltages applied to inductors L_{in} and L_i (i = 1…3) are equal to the input voltages or the string voltage V_{String}. The operation of the equalizer moves to T_{OFF} period as Q is turned off, and all the inductor currents start linearly decreasing. Applied voltages of inductors are equal to $V^*_{PVi} - V_D$ where

V^*_{PVi} is the lowest voltage of shaded modules in the string and V_D is the forward voltage of diodes — $V^*_{PVi} = V_{PV3}$ in the case shown in Figs.5 and 8.

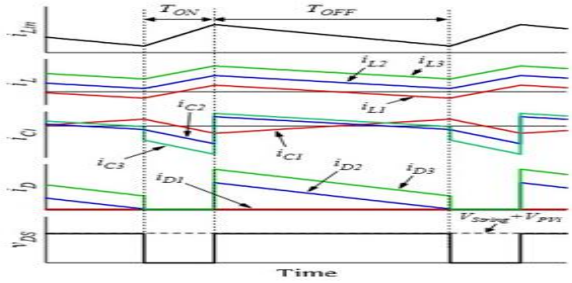

Figure.5. Operation waveform in CCM when PV2 and PV3 are moderately and severely shaded

The volt-second balance on inductors under a steady-state condition yields the voltage relationship between V_{String} and V^*_{PVi} as

$$V^*_{PVi} = \frac{D}{1-D} V_{String} - V_D \quad (1)$$

Where D is the duty cycle of the switch Q. D is adjusted so that the voltage difference (ΔV) between the measured highest and lowest module voltages (V_H and V_L, respectively) in the string to be a certain fixed value. Diodes connected to the shaded modules of PV2 and PV3 (i.e., D2 and D3) conduct, whereas that corresponding to the unshaded module of PV1 (D1) is still off, as shown in Fig. (). From Kirchhoff's current law, an equalization current supplied to PVi, I_{eqi}, is equal to an average current of L_i or D_i (I_{Li} or I_{Di}) because an average current of Ci must be zero under a steady-state condition;

$$I_{eqi} = I_{Li} = I_{Di}. \quad (2)$$

Since D1 does not conduct under this shading condition, no equalization current is supplied to the unshaded module PV1, and therefore, the average current of L_1, I_{L1}, is zero although a current ripple exists in i_{L1}. The operation waveforms in DCM are shown in Fig.6.

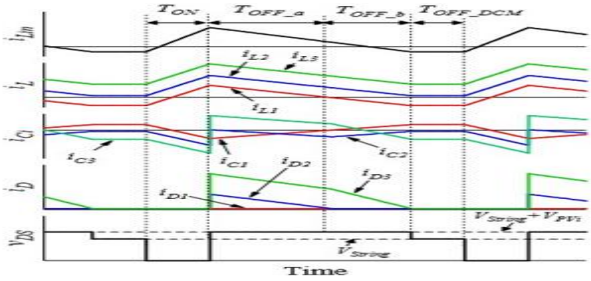

Figure.6. The operation waveforms in DCM when PV2 and PV3 are moderately and severely shaded

The current flow directions in T_{ON} and T_{OFF_a} in DCM are identical to those in T_{ON} and T_{OFF} in CCM, respectively, while the period of T_{OFF_DCM} is unique to the DCM operation. In T_{OFF_DCM} period, all the diode cease to conduct, and all the inductor currents become constant, indicating the applied voltages of inductors are zero. Similar to the CCM, the voltage relationship between V_{String} and V^*_{PVi} can be expressed as

$$V^*_{PVi} = \frac{D}{D_{ab}} V_{String} - V_D \quad (3)$$

Where D_{ab} is the duty cycle of the sum of T_{OFF_a} and T_{OFF_b} periods in DCM, as designated in Fig. 6. The boundary between CCM and DCM can be established based on whether all diode currents reach zero in switch-off state. In other words, if D_{ab} is shorter than 1 – D (i.e., $D_{ab} < 1 - D$), the operation falls into DCM. The critical duty cycle $D_{Critical}$ can be yielded as

$$D_{Critical} = \frac{V^*_{PVi} + V_D}{V_{String} + V_{PVi} + V_D}. \quad (4)$$

In order to effectively preclude the negative impacts caused by partial shading, the equalizer needs to be properly controlled with minimizing power conversion loss in the equalizer. Although voltage equalization does not guarantee that all the modules operate at each MPP, the loss in energy yield is reportedly satisfactory small and less than 2% below the ideal individual MPPT. The proposed single-switch equalizer is basically a single-input multi-output power source with one control freedom (i.e., duty cycle). In order to equalize

(or supply equalization currents to) multiple PV modules with single one control freedom, the equalizer should be operated with a proper equalization strategy. Depending on strategies, there are three conceivable equalization scenarios. For the sake of clarity, the equalizer is illustrated as a multi- output power source of V_e having respective equivalent output resistors Rout and output diodes. The relationship between the shaded module's voltage V^*_{PVi} and V_e can be yielded as

$$V^*_{PVi} = V_e - I_{eqi} R_{out} - V_D . \quad (5)$$

From (1) and (5)

$$V_e = \frac{D}{1-D} V_{String} - I_{eqi} R_{out} \approx \frac{D}{1-D} V_{String} \quad (6)$$

Indicating that V_e is essentially duty-controllable.

Equalization scenarios: There are three conceivable equalization scenarios: in sufficient equalization, over equalization and optimum equalization. The operation points of each PV substring under a partially shaded condition, where PV1 and PV2 are severely and moderately shaded, respectively, under the three equalization scenarios are shown in Fig.7.

For the sake of simplicity, the voltage equalizer in Fig.7, is equivalently illustrated as a multi output voltage source producing uniform output voltage of V_e with ideal diodes.

a) Insufficient equalization ($V_{PV1} = V_e < V_{PV2} < V_{PV3}$ or $V_{PV1} = V_{PV2} = V_e < V_{PV3}$): If the power supplied for the shaded substrings is insufficient to equalize all substring voltages, the operation is subject to insufficient equalization. The insufficient equalization for the example partially shaded condition can be subdivided into Cases1 and 2, according to the voltage relationship between V_e and $V_{PV1}-V_{PV3}$.

In Case 1 ($V_e = V_{PV1} < V_{PV2} < V_{PV3}$) shown in Fig.7(a), PV2 and PV3 receive no current from the equalizer, their currents are equal to IS tring, and they operate at respective voltage levels, which exceed V_{PV1}. Meanwhile, the equalizer supplies an equalization current of I_{eq1} for the severely shaded substring of PV1, but the power supplied for PV1 is insufficient to boost V_{PV1} to other substringvoltagelevels.AsshowninFig.7(a), the difference between I_{String} and generated current of PV1 (i.e., I_{PV1}) corresponds to I_{eq1}, as expressed by (1). Since individual PV substring operates at totally different voltage levels, the overall string operates in a voltage-mismatched condition and partial shading issues would remain.

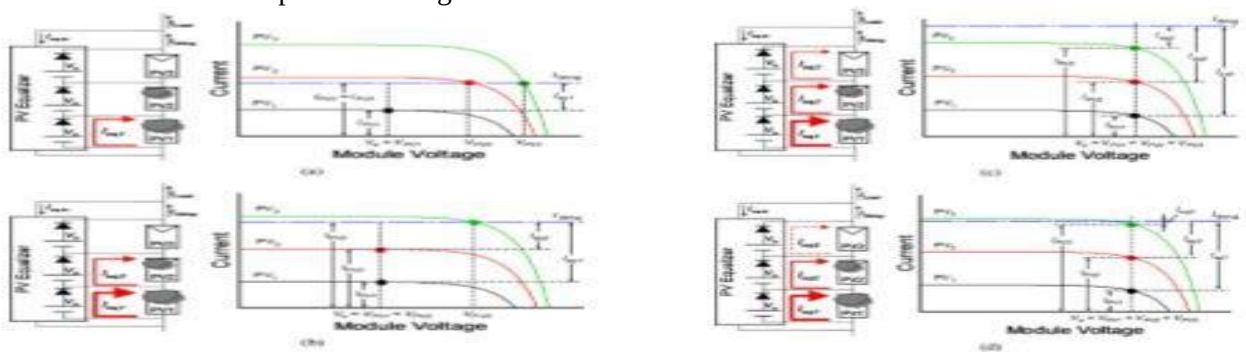

Figure.7. Operating under different equalizer scenarios (a) insufficient equalization case 1, (b) insufficient equalization case 2, (c) over equalization, (d) optimum equalization

In Case 2 ($V_e = V_{PV1} = V_{PV2} < V_{PV3}$) shown in Fig.7(b), the equalizer is more capable of supplying power for shaded substrings than in Case 1, but remains insufficient to equalize all voltages. The equalizer supplies currentsforboththeshadedsubstringsofPV1 andPV2; hence V_{PV1} and V_{PV2} are equal. However, the power supplied for PV1 and PV2 remains insufficient for their voltages of V_{PV1} and V_{PV2} to reach V_{PV3}, resulting in a voltage mismatch as $V_e = V_{PV1} = V_{PV2} < V_{PV3}$.

b) Over equalization ($V_e = V_{PV1} = V_{PV2} = V_{PV3}$): In this scenario, the voltage equalizer supplies equalization currents for not only the shaded substrings but also those unshaded, so that all substring voltages are equalized as $V_e = V_{PV1} = V_{PV2} = V_{PV3}$, as shown in Fig.7(c). With the support of the voltage equalizer, all the substrings virtually exhibit equivalent characteristics when illustrated in I_{String} versus V_{PVi} characteristics, and therefore, partial shading issues would be precluded. The apparent I_{String} is rather larger than even the unshaded substring's current of I_{PV3}, indicating that the unshaded substring of PV3 needlessly receives the relatively large equalization current of I_{eq3}; I_{String} is the sum of I_{PVi} and I_{eq-i}. A fraction of I_{String} is used as I_{eq-in} that is then converted and redistributed to each substring as $I_{eq1}-I_{eq3}$. The larger the value of I_{eq-in} or I_{eq-i} under the over equalization scenario, the larger the value of I_{String} will be, needlessly increasing processed power as well as power

conversion loss in the voltage equalizer. Therefore, to eliminate unnecessary power conversion loss in the equalizer, equalization should be performed such as to minimize the unnecessary equalization current for the unshaded substring. Equalization currents are supplied to all modules including the unshaded module PV1; a difference between I_{String} and I_{PVi} corresponds to an equalization current I_{eqi}, as designated in the figure. Since all the output diodes of the equalizer conduct, all the module voltages are equalized as $V_e - V_D = V_{PVi}$ if voltage drops across Rout are neglected. However, the unshaded module PV1 unnecessarily receives an equalization current, increasing the processed power as well as power conversion loss in the equalizer.

c) Optimum equalization ($V_e = V_{PV1} = V_{PV2} = V_{PV3}$): This scenario equates to the boundary between over equalization and the insufficient equalization in Case 2. Both the voltage relationship and the current paths are similar to those under the over equalization scenario; the equalizer supplies equalization currents for all substrings, including unshaded, so that all substring voltages are equalized as $V_e = V_{PV1} = V_{PV2} = V_{PV3}$.The difference from the over equalization scenario is that the current supplied for the unshaded substring of PV3, I_{eq3}, is minimized to nearly zero, as shown in Fig.7(d), to reduce processed power as well as power conversion loss in the equalizer. As can be compared with Fig.7(c), minimizing I_{eq3} also reduces I_{eq1} and I_{eq2}, while the operational substring voltages are identical to those under the over equalization.

Operation of equalizer: The system consists of shaded PV array, blocking diode and voltage equalization circuit. Input voltage of the equalizer circuit is obtained from the output of the PV string voltage. The multioutput of this circuit is connected across each PV panel. The circuit consists of PV string capacitance (CIN), input inductor (LIN), MOSFET switch (Q), energy transfer capacitor (C3), output inductor (L3) and output filter capacitor (COUT3). The equalizer circuit is equivalent to that of conventional SEPIC converter and filter components. The three set of filter components namely, (COUT1, L1, D1, C1), (COUT2, L2, D2, C2) and (COUT3, L3, D3, C3) represent the multi stage configuration. The advantages of this circuit include the usage of single switch, simple and easy to control. This circuit can be operated either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In this work, DCM mode is used as it eliminates the feedback control and limits the currents in the circuit with desired level. Voltage equalization circuit performs a dc conversion function. It can either increase or decrease the magnitude of the dc voltage. For analysing the configuration, consider three series connected PV panels with different irradiation levels. The equalizer configuration is operating in DCM for eliminating the feedback loop. The circuit operates in three modes which are explained below:

MODE-1(T_{ON}): During mode-1(Fig.8(a)), the switch (Q) is in ON position; the output of series connected PV panels supply the power to the voltage equalization circuit.

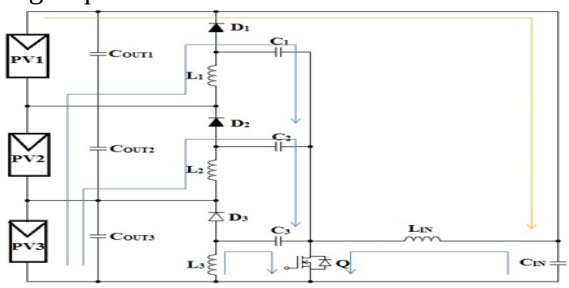

Figure.8(a). Flow of currents in Mode 1 when switch Q is in On position (T_{ON})

During this period, currents of all inductors (L1, L2 and L3) in equalization circuit increases and the inductors store the corresponding energies. The current flowing through LIN and CIN also flows towards the switch (Q). MODE-2(TOFF -a): During mode-2 (Fig.8(b)), the switch (Q) is OFF.

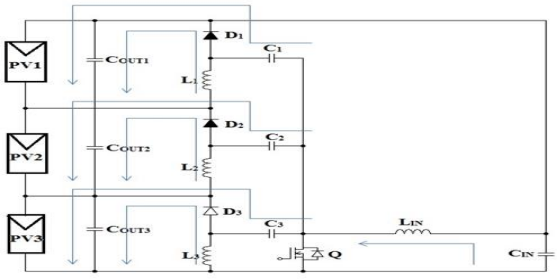

Figure.8(b). Flow of currents Mode 2 when switch Q is in Off position(T_{OFF-a})

During this period, the diode corresponding to lowest voltage PV panel-3 will get forward biased. Hence, the stored energies in the inductors (L1, L2 and L3) transferred to that PV module.

MODE-3(TOFF -b): During mode-3 (Fig. 8(c)), switch (Q) and diodes (D1, D2 and D3) are in OFF position. During this VIN(min) = minimum input voltage period, inductor currents are constant and equal to zero and therefore the inductor voltage must be zero.

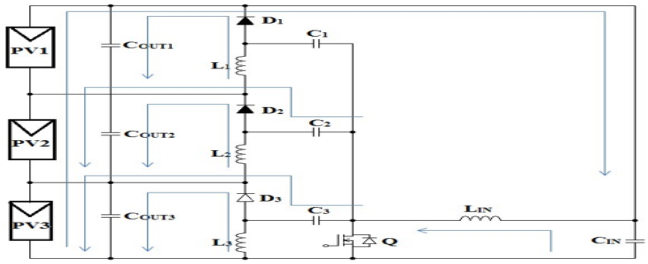

Figure.8(c). Flow of currents Mode 3 when switch Q& diodes are in Off position(TOFF-b)

After the current of diode (D3) falls to zero, the currents in the equalizer inductors become constant or zero. In multi-stage SEPIC circuit, the average currents of D1, D2 and D3 are equal to average currents of IL1, IL2 and IL3 respectively. Therefore, the average currents of L1, L2 and L3 are zero and only ripple current will flow through these inductors. As the large power generated by unshaded panels is transferred to the low illuminated panel through multi-stage SEPIC equalizing circuit, slowly imbalance of PV panel voltages vanishes.

Each PV equalizer is based on one of the buck–boost converters with stacked CLD filters. In all proposed equalizer topologies, an asymmetric square-wave voltage is produced across the switch Q and capacitors C1–C3 act as coupling capacitors, allowing only the component to flow through. Although the stacked CLD filters have different dc voltage levels, the same asymmetric square voltage wave is applied to all inductors L1−L3 due to the coupling, producing a uniform output voltage for each PV substring. Although equalizers are for a panel consisting of three substrings, the propose voltage equalizers can be applied to any number of substrings/modules; the equalizers can be extended by increasing the number of stacked CLD filters and adjusting component rating.

Component rating:

Calculate maximum switch current: For calculating the switch current we have to calculate duty cycle D for the minimum input voltage. The minimum input voltage is used because this leads to the maximum switch current.

$$D = 1 - \frac{V_{IN(min)} \times \eta}{V_{OUT}} \quad (7)$$

V_{OUT} = desired output voltage, η = efficiency of the converter, e.g. estimated 80%.

The efficiency is added to the duty cycle calculation, because the converter has to deliver also the energy dissipated. This calculation gives a more realistic duty cycle than just the equation without the efficiency factor. The next step to calculate the maximum switch current is to determine the inductor ripple current.

$$\Delta I_L = \frac{V_{IN(min)} \times D}{f_S \times L} \quad (8)$$

$V_{IN(min)}$ = minimum input voltage, D = duty cycle, f_S = minimum switching frequency of the converter L = selected inductor value.

$$I_{MAXOUT} = \left(I_{LIM(min)} - \frac{\Delta I_L}{2}\right) \times (1-D) \quad (9)$$

$I_{LIM(min)}$ = minimum value of the current limit of the integrated switch, ΔI_L = inductor ripple current, D = duty cycle calculated.

If the calculated value for the maximum output current of the selected IC, I_{MAXOUT}, is below the systems required maximum output current, another IC with a higher switch current limit has to be used. Only if the calculate value for I_{MAXOUT} is just a little smaller than the needed one, it is possible to use the selected IC with an inductor with higher inductance if it is still in the recommended range. A higher inductance reduces the ripple current and therefore increases the maximum output current with the selected IC. If the calculated value is above the maximum output current of the application, the maximum Switch current in the system is calculated:

$$I_{SW(max)} = \frac{\Delta I_L}{2} + \frac{I_{OUT(max)}}{1-D} \quad (10)$$

ΔI_L = inductor ripple current; $I_{OUT(max)}$ = maximum output current necessary in the application; D = duty cycle.

This is the peak current, the inductor, the integrated switch (es) and the external diode has to withstand.

Inductor selection: The higher the inductor value, the higher is the maximum output current because of the reduced ripple current. The lower the inductor value, the smaller is the solution size. the inductor must always have a higher current rating than the maximum current given because the current increases with decreasing inductance.

The following equation is a good estimation for the right inductor:

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_L \times f_S \times V_{OUT}} \quad (11)$$

V_{IN} = typical input voltage; V_{OUT} = desired output voltage; f_S = minimum switching frequency of the converter; ΔI_L = estimated inductor ripple current.

The inductor ripple current cannot be calculated because the inductor is not known. A good estimation for the inductor ripple current is 20% to 40% of the output current.

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{OUT(max)} \times \frac{V_{OUT}}{V_{IN}} \quad (12)$$

ΔI_L = estimated inductor ripple current; $I_{OUT(max)}$ = maximum output current necessary in the application.

Rectifier diode selection: To reduce losses, Schottky diodes should be used. The forward current rating needed is equal to the maximum output current:

$$I_F = I_{OUT(max)} \quad (13)$$

I_F = average forward current of the rectifier diode, $I_{OUT(max)}$ = maximum output current necessary in the application.

Schottky diodes have a much higher peak current rating than average rating. Therefore the higher peak current in the system is not a problem.

The other parameter that has to be checked is the power dissipation of the diode. It has to handle:

$$P_D = I_F \times V_F \quad (14)$$

I_F = average forward current of the rectifier diode; V_F = forward voltage of the rectifier diode.

Output capacitor selection: Best practice is to use low ESR capacitors to minimize the ripple on the output voltage. Ceramic capacitors are a good choice if the dielectric material is X5R or better.

If the converter has external compensation, any capacitor value above the recommended minimum can be used, but the compensation has to be adjusted for the used output capacitance.

With internally compensated converters, the recommended inductor and capacitor values should be used or the recommendations for adjusting the output capacitors to the application should be followed for the ratio of L × C. With external compensation, the following equations can be used to adjust the output capacitor values for a desired output voltage ripple.

$$C_{OUT(min)} = \frac{I_{OUT(max)} \times D}{f_S \times \Delta V_{OUT}} \quad (15)$$

$C_{OUT(min)}$ = minimum output capacitance; $I_{OUT(max)}$ = maximum output current of the application; D = duty cycle; f_S = minimum switching frequency of the converter; ΔV_{OUT} = desired output voltage ripple.

The ESR of the output capacitor adds some more ripple, given with the equation:

$$\Delta V_{OUT(ESR)} = ESR \times \left(\frac{I_{OUT(max)}}{1-D} + \frac{\Delta I_L}{2} \right) \quad (16)$$

$\Delta V_{OUT(ESR)}$ = additional output voltage ripple due to capacitors ESR; ESR= equivalent series resistance of the used output capacitor; $I_{OUT(max)}$ = maximum output current of the application; D = duty cycle; ΔI_L = inductor ripple current.

Modelling and Simulation: In our simulation, we are using three PV modules connected in series as shown in Fig.9. The simulation is done using MATLAB SIMULINK.

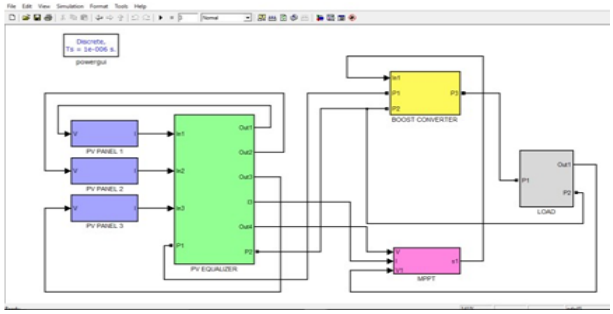

Figure9. Simulation block diagram of the proposed system

The voltage equalizer circuit diagram with mulistacked buck-boost converter is shown below in Fig.10.

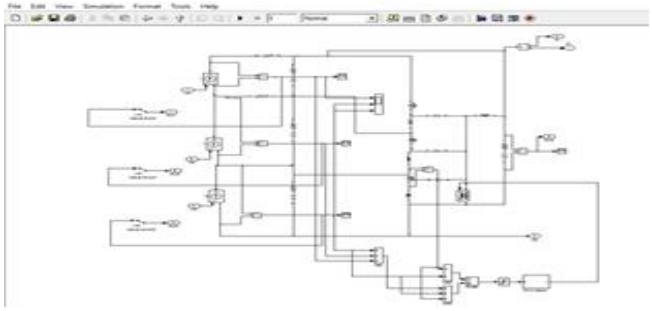

Figure.10. Simulation circuit diagram of voltage equalizer

The MPPT simulation diagram with the coding used for MPPT algorithm is shown in Fig.11.

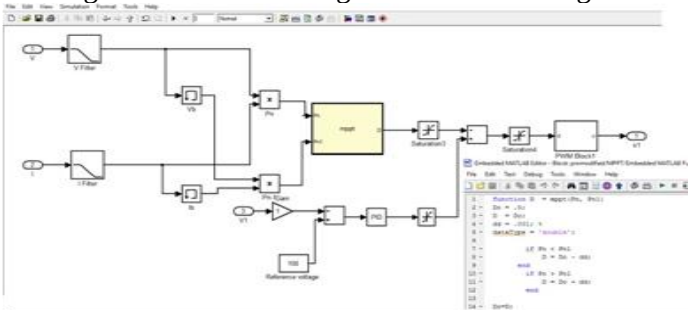

Figure.11. Simulation diagram of MMPT block with coding for MMPT algorithm

The equalized voltage waveform is shown in fig.12.

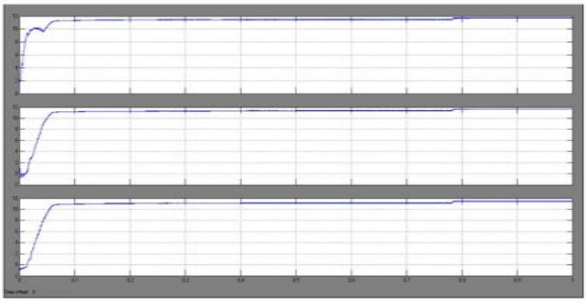

Figure.12. Equalized voltage waveform

The output voltage waveform is shown in fig.13.

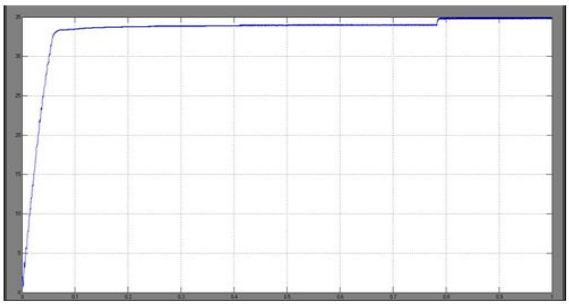

Figure.13. Output voltage waveform

The boosted o u t p u t voltage waveform f r o m t h e boost converter is shown below in fig.14.

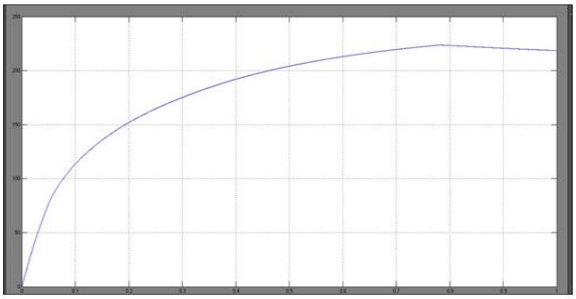

Figure.14. Boosted output voltage waveform

Hardware: The circuit diagram for the hardware setup is shown below in Fig.15.

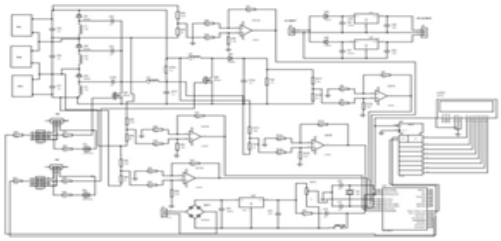

Figure.15. Circuit diagram of the hardware setup

The photo of the hardware setup is shown below in fig.16. The main modules used in the hardware unit are partially shaded PV module which is done using different transformer supply, voltage equalizer unit, boost converter unit, gate driver circuit, RPS unit, MPPT unit and load.

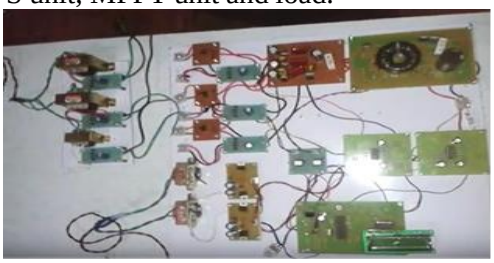

Figure.16. Hardware setup of the proposed system

4. CONCLUSION

Single-switch voltage equalizers for partially shaded PV modules have been proposed in this paper. The proposed voltage equalizers can be derived by stacking CLD filters on traditional buck–boost converters, such as SEPIC, Zeta, and CUK converters. The single switch topology can simplify the circuitry compared with conventional converters and voltage equalizers requiring numerous switches proportional to the number of PV substrings/modules in series. Depending on the equalization strategies, the proposed voltage equalizers might supply excessive equalization currents for un shaded substrings, needlessly increasing power conversion loss. The optimum equalization strategy, with which equalization currents for un shaded substrings are minimized, was proposed and discussed for the equalizers to work efficiently. Operational analyses based on the simplified equivalent circuit were also performed for the SEPIC-based equalizer, and a control circuit that substantiates the optimum equalization strategy was also introduced.

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